How to Increase Output Current Capability Using Load Sharing Method

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Introduction

Power demand in portable designs can require in some specific application more than 1 A. A method consists in paralleling two DC to DC converters on the same load instead of placing a single higher current converter with lower switching frequency. This solution may be space saving, cost effective and thermally beneficial.

However, DC to DC converters regulate their own output voltage with a tolerance which includes bandgap deviation, comparator offsets and closed loop regulation parameters. Using converters with external resistor bridge implies to also take into consideration resistor accuracies. This application note will detail the tips and tricks to implement load sharing method with NCP1532.

The NCP1532 dual step down DCDC converter includes two channels externally adjustable from 0.9 V to 3.3 V which can source totally up to 1.6 A, 1.0 A maximum per channel. The MODE/SYNC pin allows to force the part in PWM mode which is required to operate with the load sharing method. Both converter can operate out of phase at 2.25 MHz or can be synchronized in phase to an external clock.

External Components Must Be Evaluated

Paralleling two DC to DC converters to increase output current capability requires additional ballast resistors to prevent the fact that the two converters are not exactly set at the same voltage. Using the NCP1532, we can consider that the deviation coming from the error amplifier and reference voltage can be negligee inside the same circuit. Handled designers must minimize these ballast resistors to reduce power looses and ensure acceptable load regulation performance.

The following assumptions have been used to calculate ballast resistors:

1. It is mandatory to force both converters in continuous or discontinuous PWM mode. Due to the nature of the PFM mode, connected output of two buck converters together can cause abnormal behavior at very light load. In this mode, switching activities events of one converter can deregulate the error amplifier of the second converter. Load sharing method supposes needed higher load current range and not required PFM mode benefits.

   NCP1532 will be synchronized in forced PWM to an external 3 MHz clock to demonstrate load sharing capabilities.

2. Both converters use the same reference voltage. However due to external resistor tolerances, each regulated output voltages are different. We can take the assumption that channel 1 regulates at the high end of its tolerance while channel 2 regulates at the low end.

$$V_{OUT1high} = V_{OUT} \times (1 + TOL_{OUT}) \qquad \text{(eq. 1)}$$

   is the channel 1 high regulation

$$V_{OUT2low} = V_{OUT} \times (1 - TOL_{OUT}) \qquad \text{(eq. 2)}$$

   is the channel 2 low regulation
   Where TOL_{OUT} is the tolerance brought by external divider, given by Equation 12.

3. Ballast resistors will ensure that both converters can not exceed their maximum output current, e.g. 1 A per channel.

$$I_{OUT1max} = I_{OUT2max} = I_{OUTmax} = 1 \text{ A} \qquad \text{(eq. 3)}$$

   is the maximum output current per channel.

$$I_{LOADmax} = I_{OUT1} + I_{OUT2} = 1.6 \text{ A} \qquad \text{(eq. 4)}$$

   is NCP1532 maximum−rated current.

4. Both R_{SHARE} ballast resistor are at the same value.

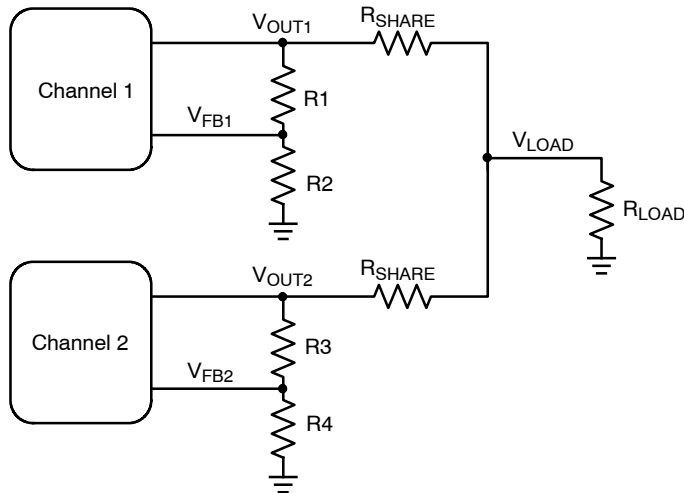$$R_{SHARE1} = R_{SHARE2} = R_{SHARE} \qquad \text{(eq. 5)}$$

Figure 1. Depicts Load Sharing Block Diagram

The electrical translation of Figure 1 block diagram is given by:

$$R_{SHARE} = \frac{V_{OUT1} - V_{OUT2}}{I_{OUT1} - I_{OUT2}} \quad \text{(eq. 6)}$$

The worst case conditions defined by assumptions (1), (2), (3) and (4) leads to following voltage / current couples:

$$\begin{cases} V_{OUT1} = V_{OUT1high} & \text{(eq. 7)} \\ I_{OUT1} = I_{OUTmax} & \text{(eq. 8)} \end{cases}$$

$$\begin{cases} V_{OUT2} = V_{OUT2low} & \text{(eq. 9)} \\ I_{OUT2} = I_{LOADmax} - I_{OUTmax} & \text{(eq. 10)} \end{cases}$$

Equation 6 gives:

$$R_{SHARE} = \frac{2.V_{OUT}.TOL_{OUT}}{2.I_{OUT} - I_{LOADmax}} \quad \text{(eq. 11)}$$

The overall output voltage reference TOL_{OUT} depends upon the accuracy of the external divider TOL_R:

$$TOL_{OUT} = 2 \times \left(1 - \frac{V_{FB}}{V_{OUT}}\right) \times TOL_R \quad \text{(eq. 12)}$$

Let us calculate ballast resistors using (11) and (12). The tolerance on the output of the DC to DC for $V_{OUT} = 1.2$ V and using resistor divider with 0.1% accuracy is:

$$TOL_{OUT} = 2 \times \left(1 - \frac{0.6}{1.2}\right) \times 0.1\% = 0.1\%$$

This leads to calculate R_{SHARE} ballast resistors:

$$R_{SHARE} = \frac{2 \times 1.2 \times 0.1\%}{2 \times 1 - 1.6} = 6 \text{ m}\Omega$$

Simulations and measurements described in next section are based on following application schematic:
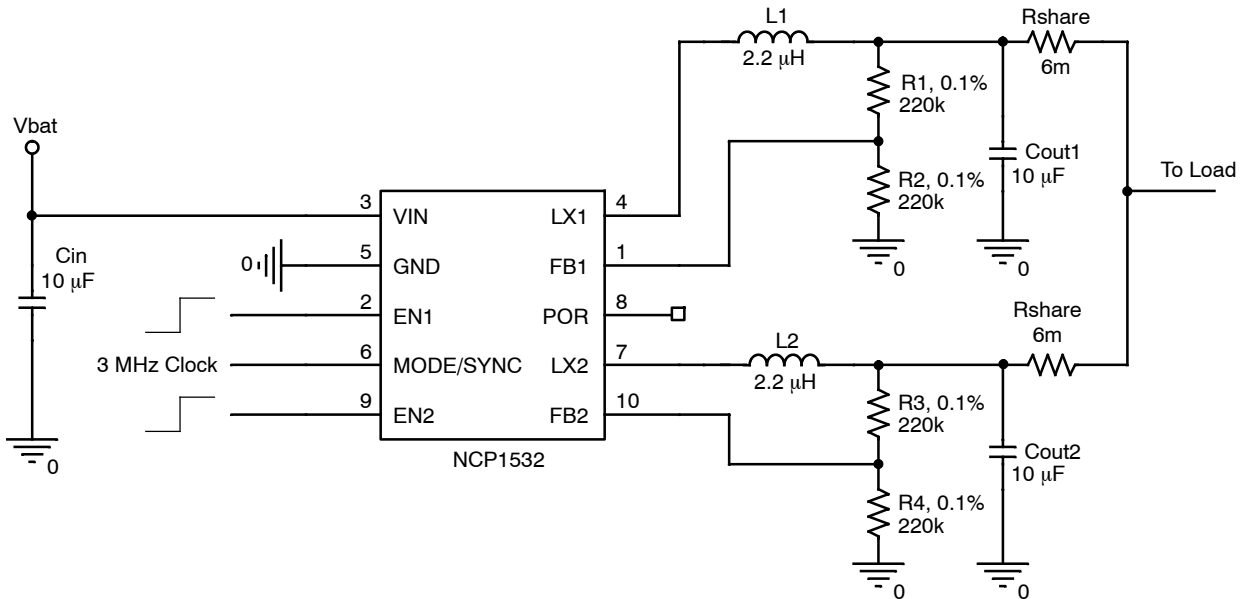
Figure 2. NCP1532 Load Sharing Application Schematic

Simulations Depict Impact On Load Regulation

If we consider the two channels as ideal voltage sources which are configured to provide 1.2 V ± their 0.1% tolerance, we can use Figure 3 to validate previous calculation results.
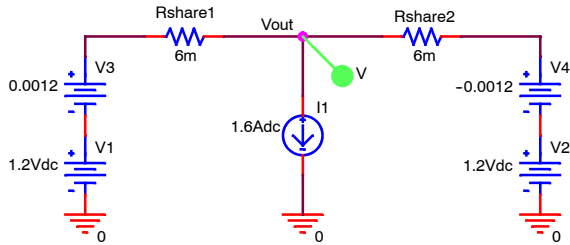

Figure 3. Represents Load Sharing Simulation

Using 6 mΩ ballast resistors compensate the high and low end tolerances of the resistor divider without exceeding NCP1532's maximum output current capability. This method, however, will impact load regulation performances up to 4.8 mV and will increase losses if ballast resistors have not been minimized by Equation 11. Figure 4 depicts load regulation from V_{out} = 1.2 V when load current increases up to 1.6 A, based on Figure 3 schematic.
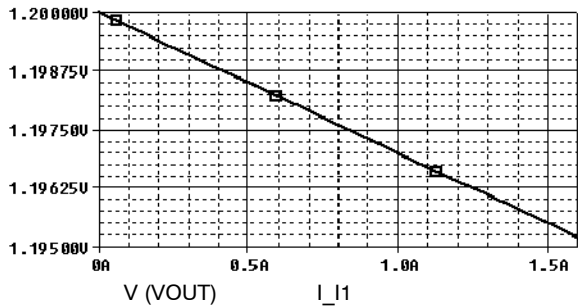
Figure 4. Shows Impact of Ballast Resistors on Load Regulation

Minimize R$_{SHARE}$ Resistor Is Key For Efficiency

Minimizing ballast resistors by Equations 11 and 12 also impact NCP1532 efficiency performance. At 1.6 A load, R$_{SHARE}$ resistive losses are given by:

$$P_{SHARE} = \left(I_{OUT1max}{}^2 + I_{OUT2}{}^2\right) \times R_{SHARE}$$

$$P_{SHARE} = (1 + 0.6^2) \times 60.10^{-3} = 82 \text{ mW}$$

In case of symmetric loading, R$_{SHARE}$ resistive losses give:

$$P_{SHARE} = \left(I_{OUT1}{}^2 + I_{OUT2}{}^2\right) \times R_{SHARE}$$

$$P_{SHARE} = 2 \times 0.8^2 \times 6.10^{-3} = 7.7 \text{ mW}$$

This can be compared to the power given to the load P$_{LOAD}$:

$$P_{LOAD} = I_{LOADmax} \times V_{LOAD}$$

$$P_{LOAD} = 1.6 \times 1.2 = 1.92 \text{ W}$$

Efficiency impact due to ballast resistors is equal or less than 0.5%.
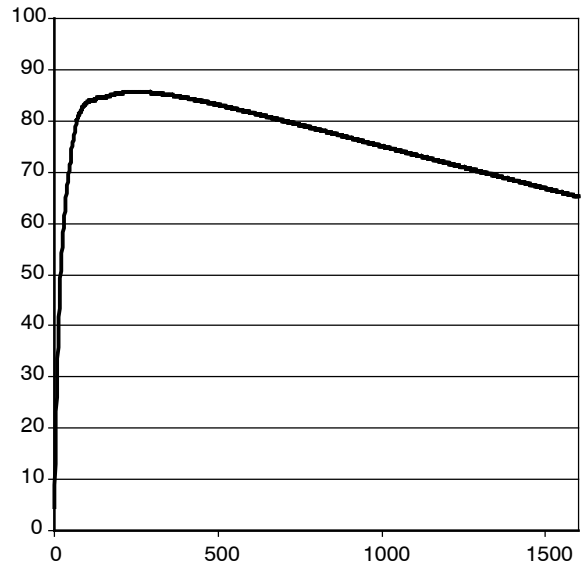
Figure 5. Represents NCP1532 Efficiency using Load Sharing Method

Load Transients Performance Validates The Design

Use of two separate channels helps to react to big load transient events. Furthermore, compared to a "super" DC to DC converter, the load sharing method allows using higher frequency devices with larger bandwidth. The high switching frequency requires smaller inductor which needs less time to react to current change. Following picture details 800 mA load transient with 1 μs rising time associated to the application circuit given by Figure 2.
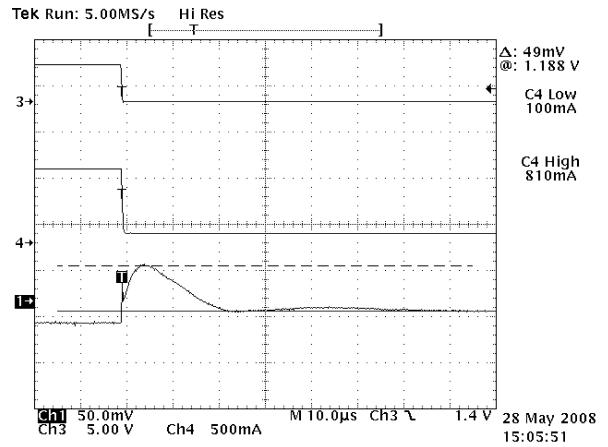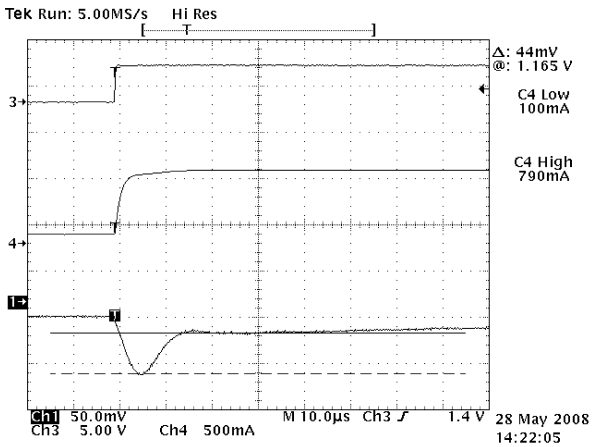
Figure 6. 0 mA to 800 mA and 800 mA to 0 mA Load Transient
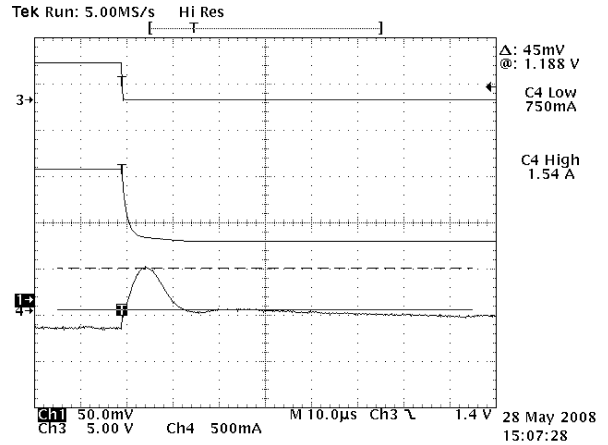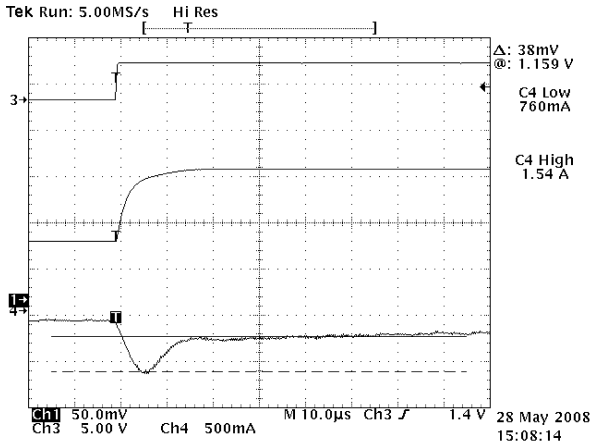
Figure 7. 800 mA to 1600 mA and 1600 mA to 800 mA Load Transient

Transient performances prove system large bandwidth and stability: Acceptable undershoot with no ringing and fast recovery. These figure give less than 50 mV drops for 800 mA load transient with 1 μs rising time. This measurement validates load sharing analysis and puts forward a main advantage of this solution

Out of Phase Operation Decreases Transient Noise on Battery Line and EMI

The NCP1532 can operate out of phase; this option is externally selectable. In that mode of control, first converter's switching event (black curve) is at the opposite (180°) of the second converter's switching event (green curve). By the way, power demand on the battery line is spread over two operating phases and the triangular form (Figure 8, left red curve) disappears using the out of phase operation (right red curve). Spikes which happen as soon as high side and low side transistors are turning ON and OFF are also considerably reduced.
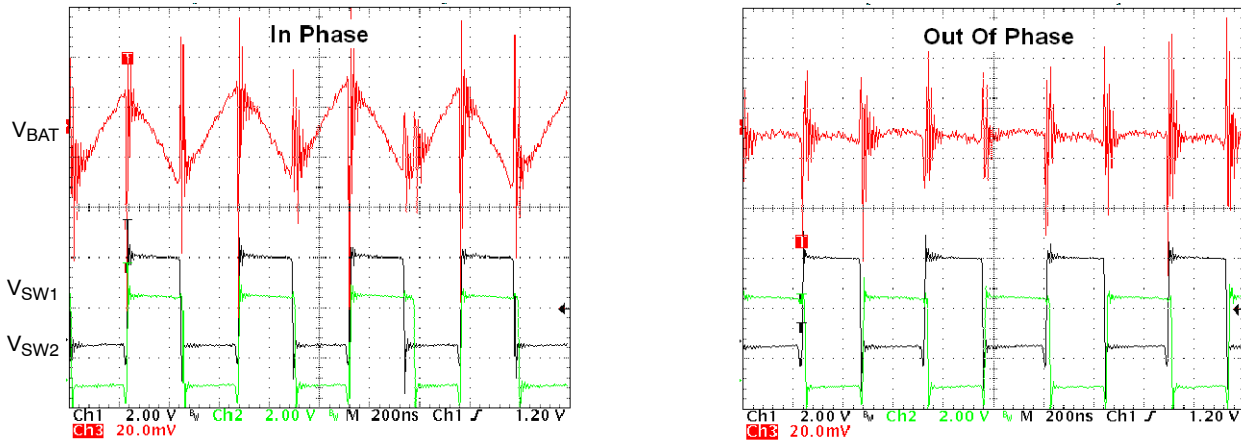
Figure 8. Pictures the Improvement of the Out Of Phase Operation on the Battery Line

Space Requirement and Layout

Implementing high frequency DC to DC converters requires respect of some rules to get a powerful portable application.

Good layout is key to prevent switching regulators to generate noise to application and to themselves. Feed back pin protection against any external parasitic signal coupling requires special care. As portable digital circuits consume a large amount of current, the loop formed by high current path from the battery to the ground plane and so called the current loop must be particularly checked by designers from the input to the output.

At least four layers PCB with ground and power planes are generally implemented. Figure 9 pictures NCP1532 load sharing recommended layout on a four-layer board. High current path (L-C filters and ballast resistors) is designed on top while sensitive feedback nets are on bottom. The solution costs 108 mm² space on top.

Figure 9. Load Sharing Application Top and Bottom View